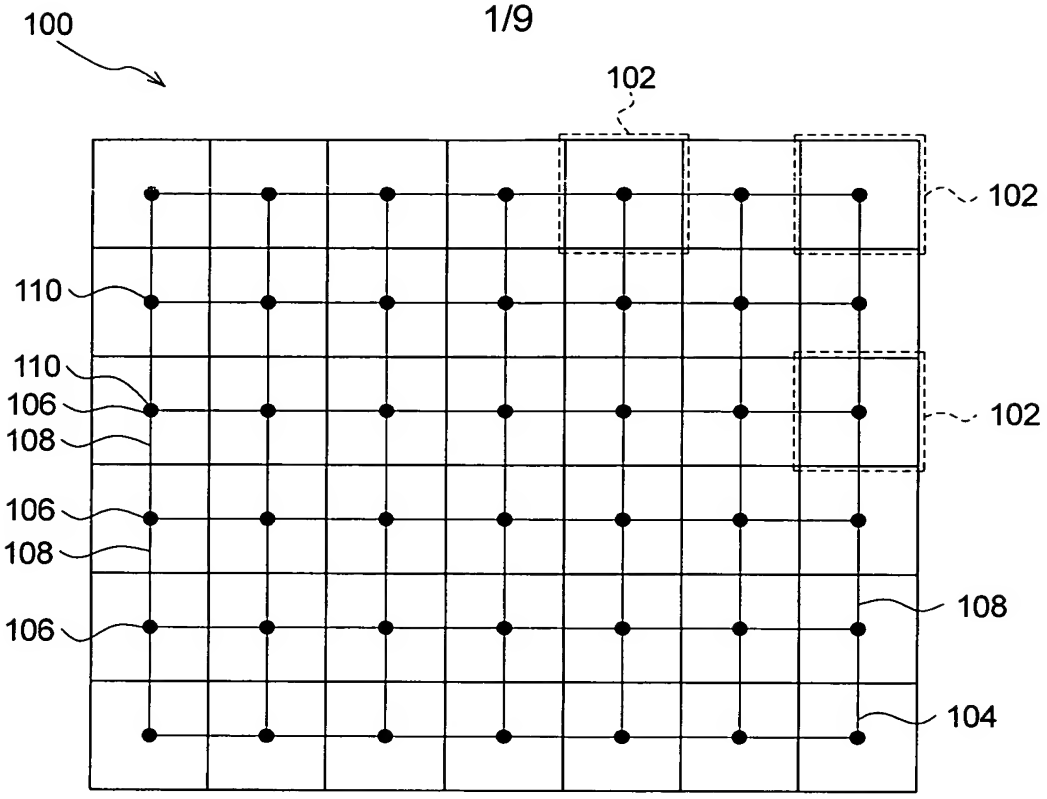
100
102
102
102
110
110
106
108
106
108
106
108
104

FIG. 1

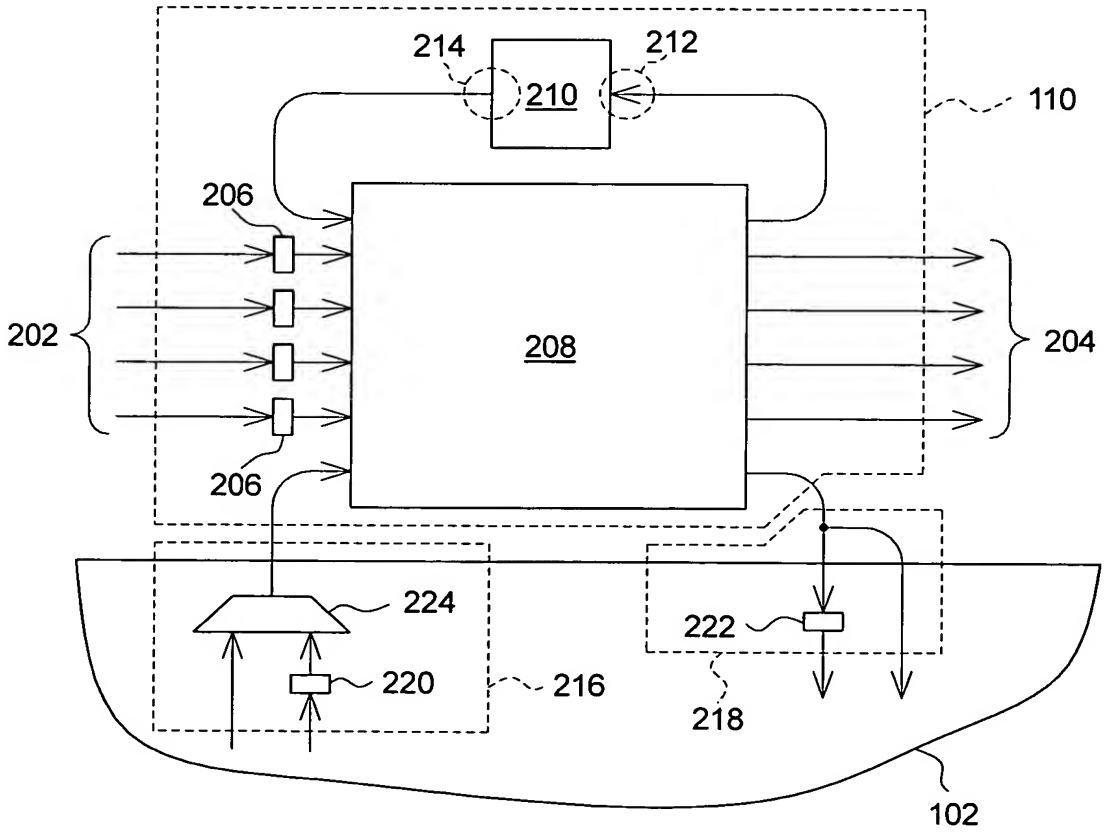
214
212
210
110
206
202
208
204
206
224
222
220
216
218
102

FIG. 2

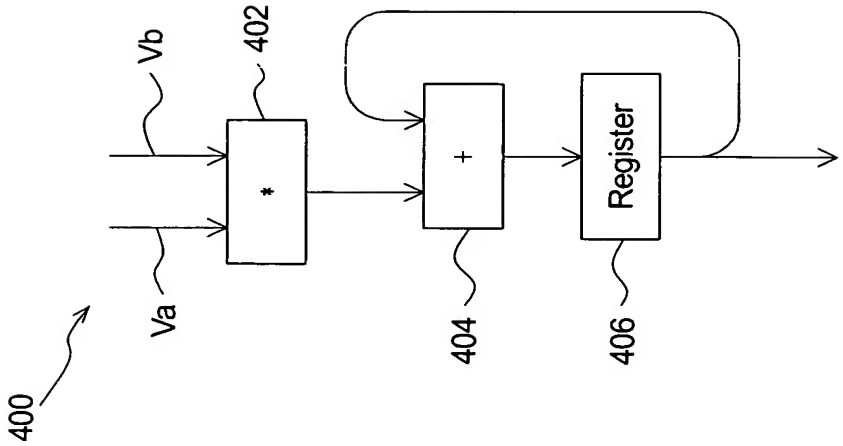
Vb
402
*
+
Register
Va
404
406
400

FIG. 4

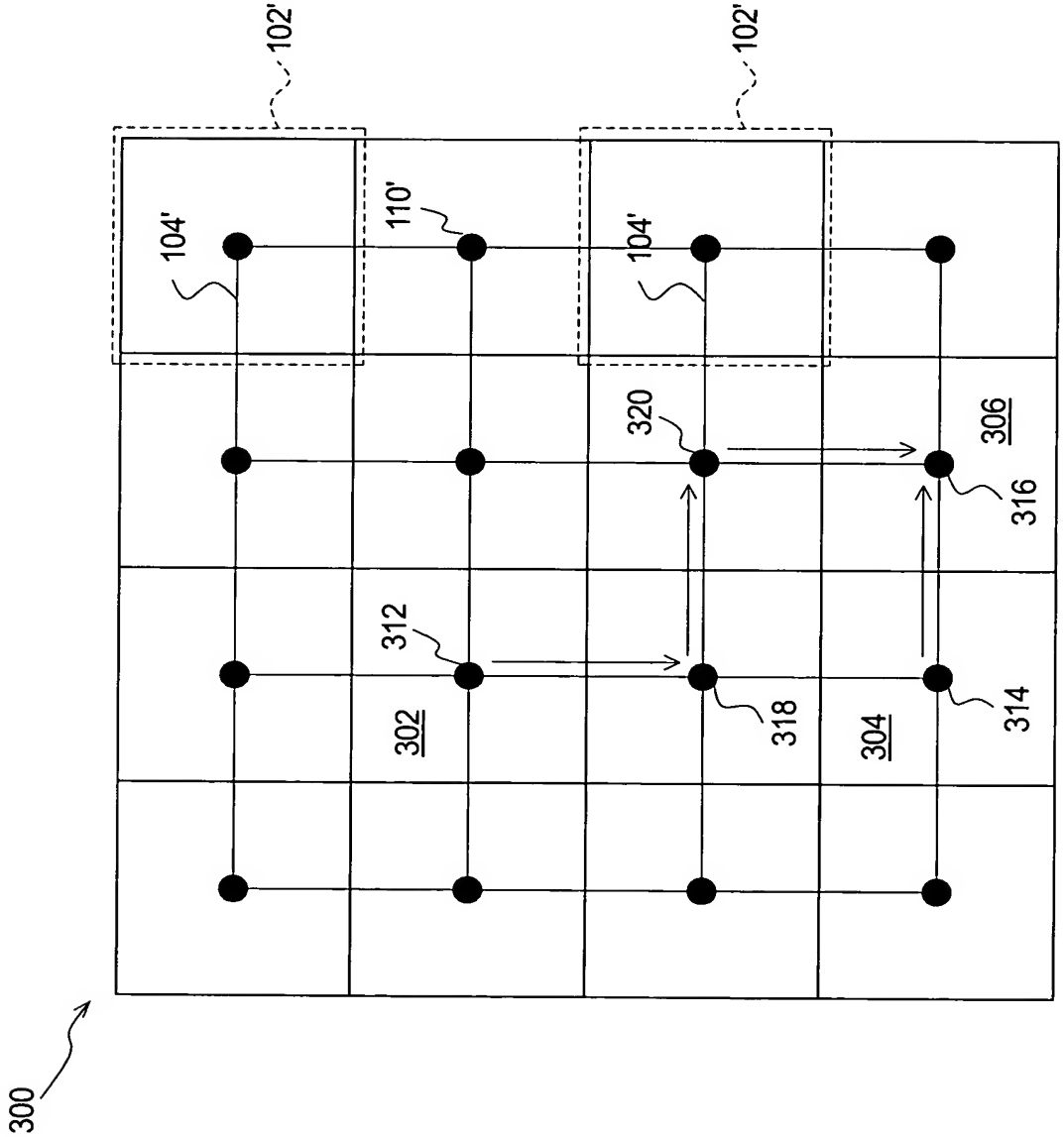
102'
102'
104'
110'
104'
320
306
316
312
302
318
304
314
300

FIG. 3

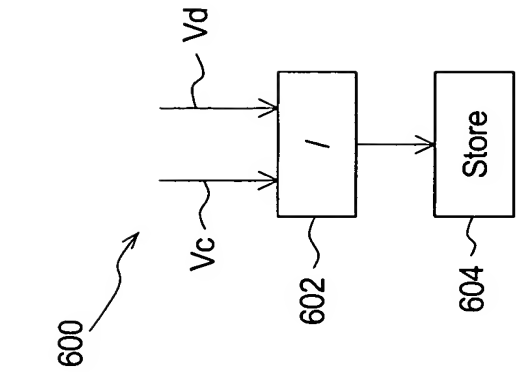

FIG. 6

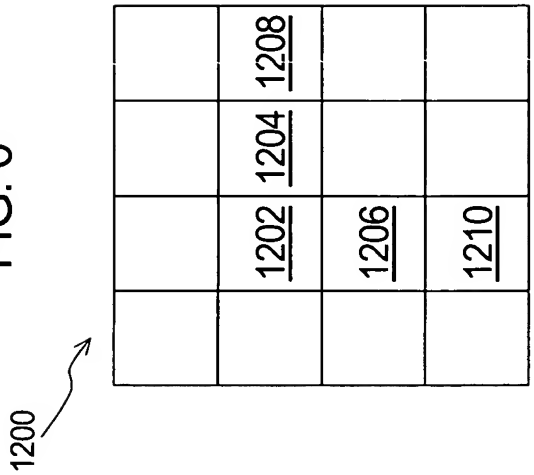

FIG. 12

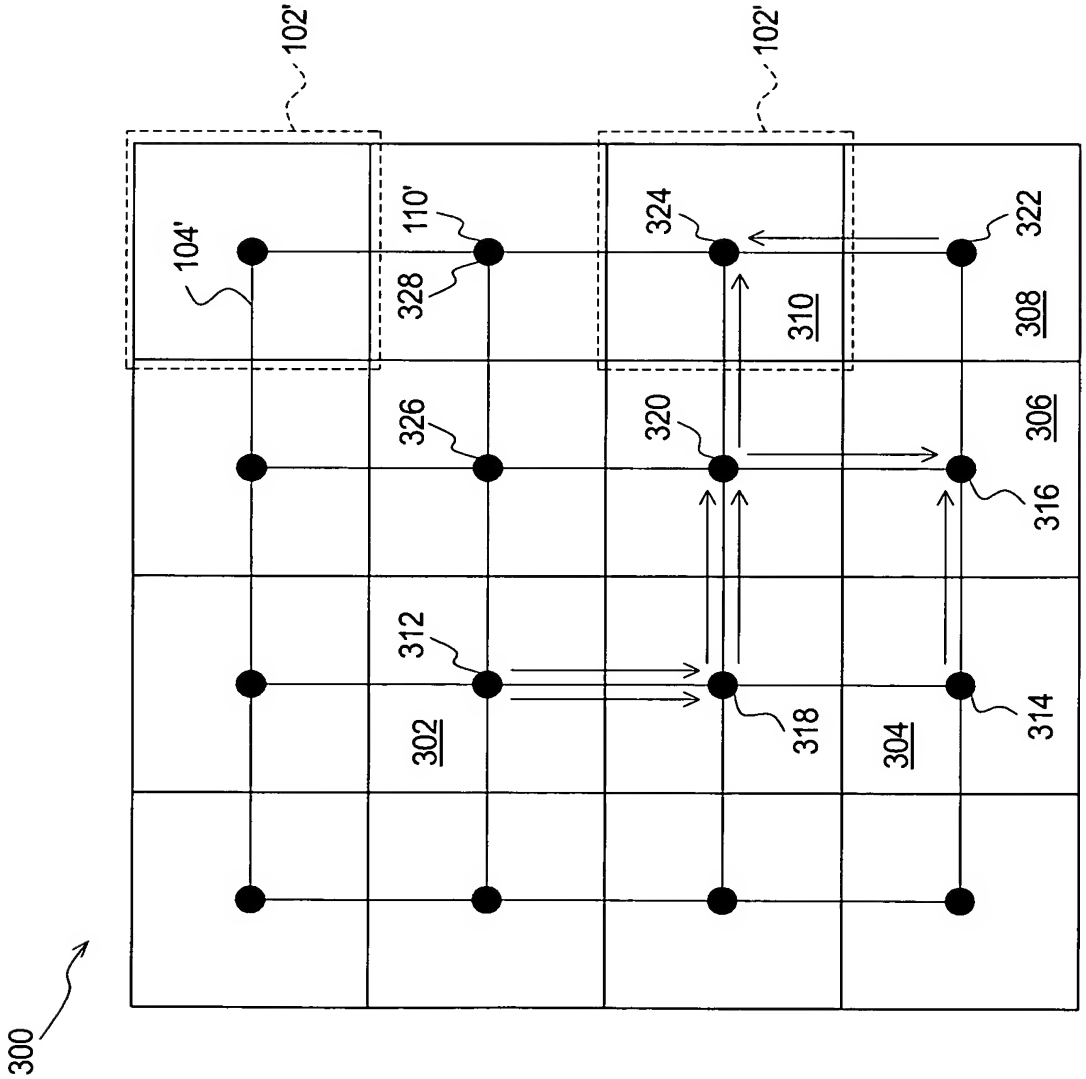

FIG. 5

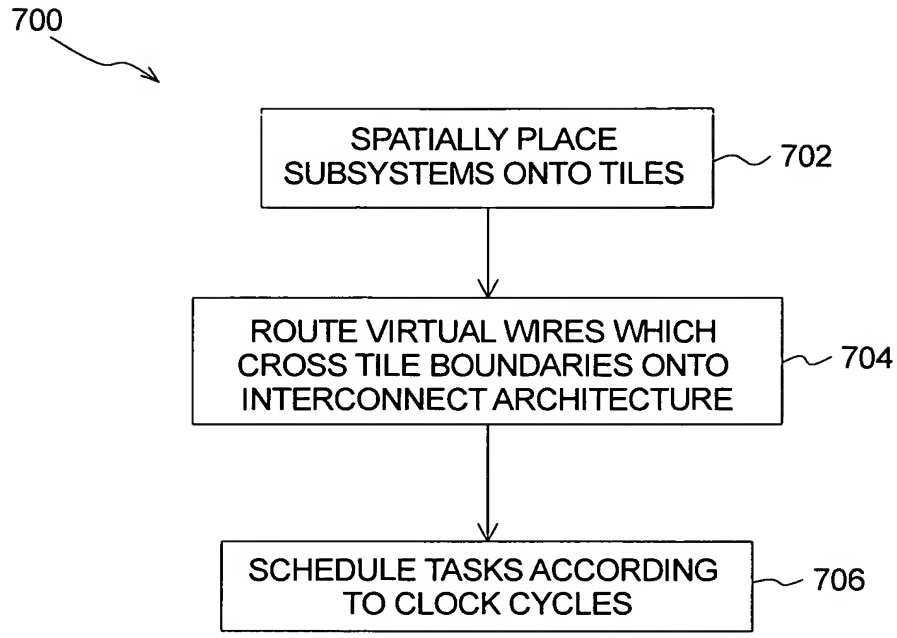
700
SPATIALLY PLACE SUBSYSTEMS ONTO TILES
702
ROUTE VIRTUAL WIRES WHICH CROSS TILE BOUNDARIES ONTO INTERCONNECT ARCHITECTURE
704
SCHEDULE TASKS ACCORDING TO CLOCK CYCLES
706

FIG. 7

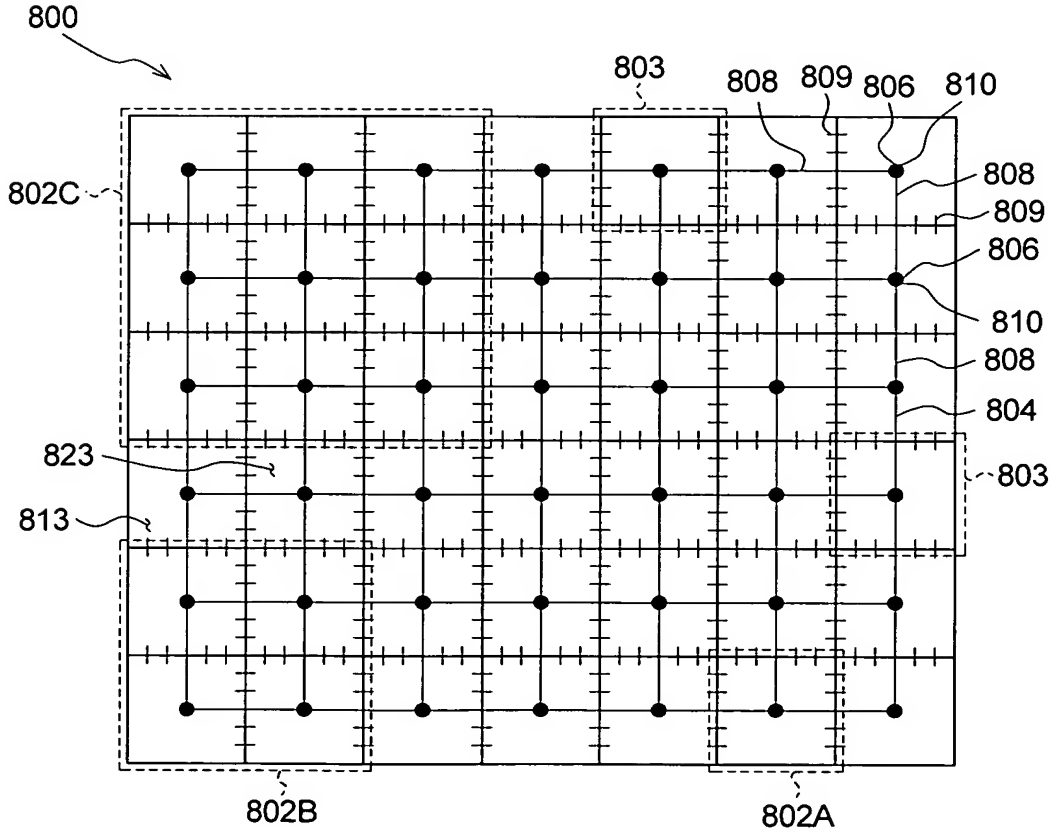
800
803
808
809
806
810
802C
808
809
806
810
808
804
823
803
813
802B
802A

FIG. 8

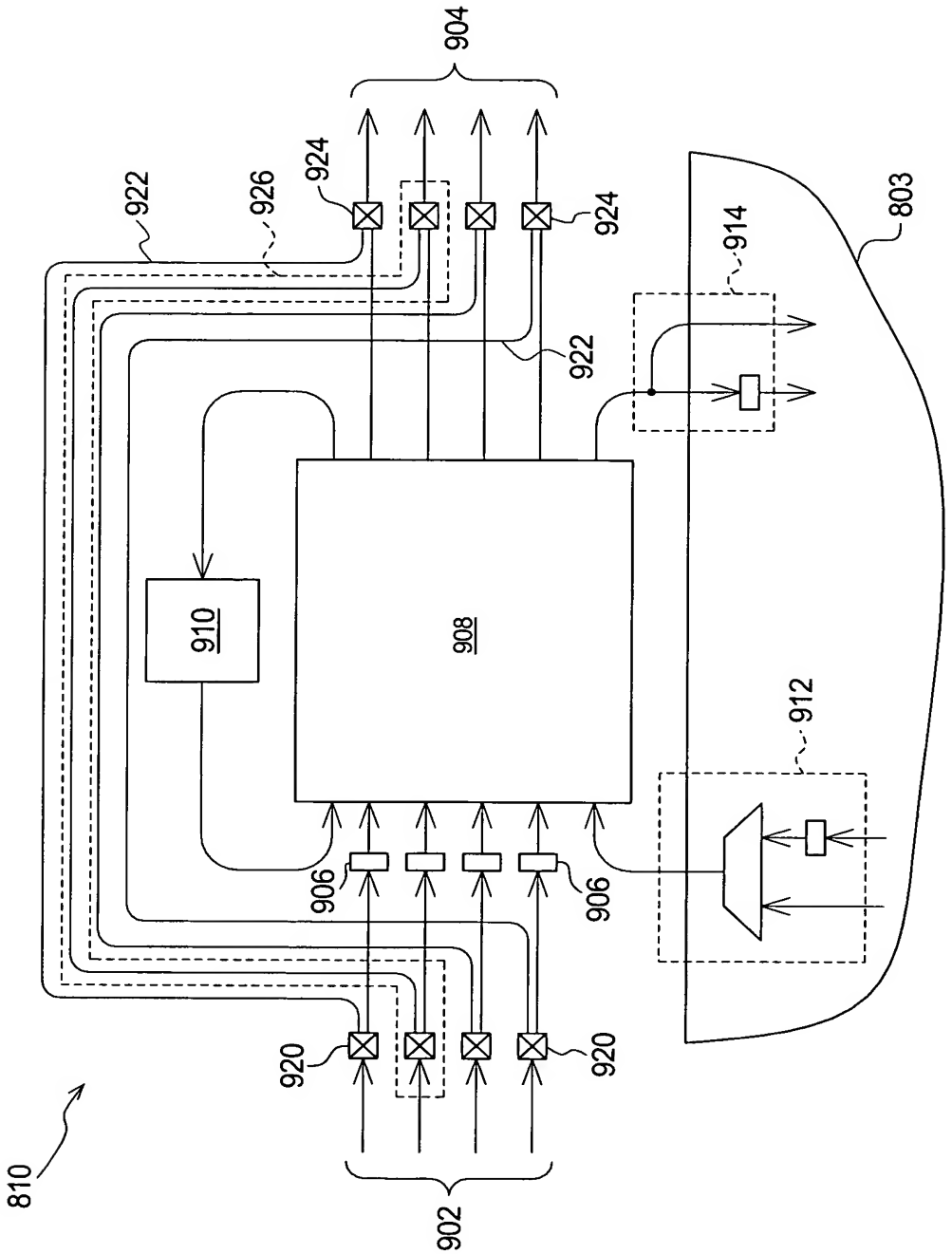
904
922
926
924
924
803
914
922
910
908
912
906
906
920
920
902
810

FIG. 9

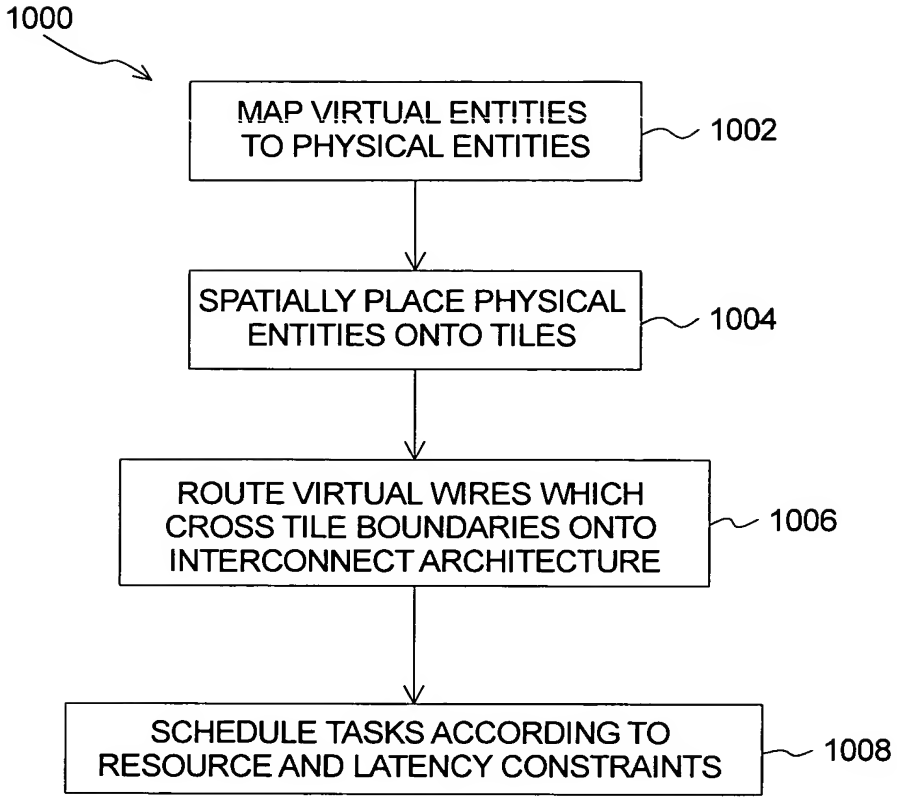
1000
MAP VIRTUAL ENTITIES TO PHYSICAL ENTITIES
1002
SPATIALLY PLACE PHYSICAL ENTITIES ONTO TILES
1004
ROUTE VIRTUAL WIRES WHICH CROSS TILE BOUNDARIES ONTO INTERCONNECT ARCHITECTURE
1006
SCHEDULE TASKS ACCORDING TO RESOURCE AND LATENCY CONSTRAINTS
1008

FIG. 10

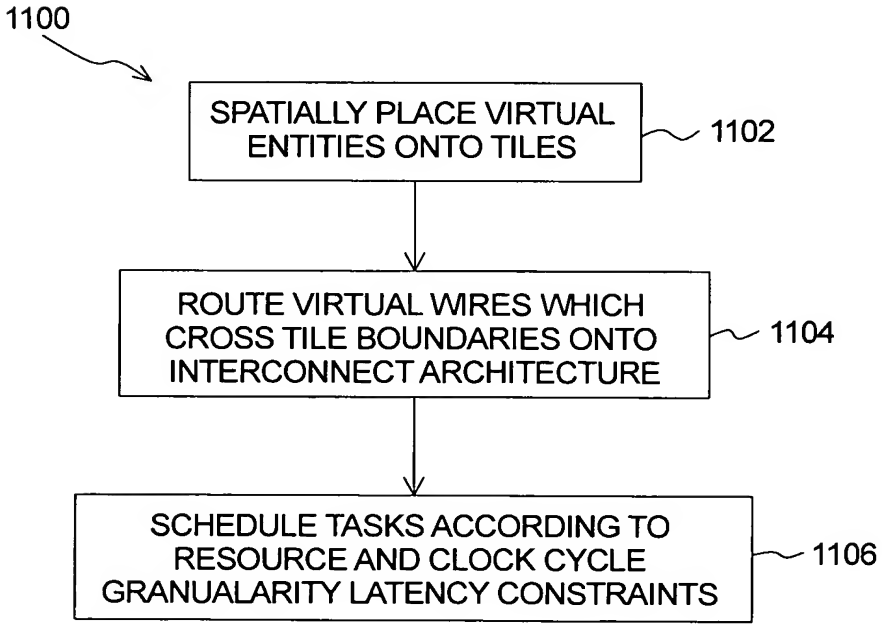
1100
SPATIALLY PLACE VIRTUAL ENTITIES ONTO TILES
1102
ROUTE VIRTUAL WIRES WHICH CROSS TILE BOUNDARIES ONTO INTERCONNECT ARCHITECTURE
1104
SCHEDULE TASKS ACCORDING TO RESOURCE AND CLOCK CYCLE GRANUALARITY LATENCY CONSTRAINTS
1106

FIG. 11

Table 3					
Time	In tile 1206	Between tiles 1202 and 1206	In tile 1202	Between tiles 1202 and 1204	In tile 1204
1			uAddr = a + 4		
2			wAddr = b + 8	uAddr transfers from 1202 to 1204	
3		wAddr transfers from 1202 to 1206	r = a + b		u = load(uAddr)
4	w = load(wAddr)		s = 5 + c	u transfers from 1204 to 1202	
5		w transfers from 1206 to 1202	x = u + r		
6			y = w + s		
7			z = s + r		

FIG. 13

Table 4					
Time	In tile 1206	Between tiles 1202 and 1206	In tile 1202	Between tiles 1202 and 1208	In tile 1208
1			uAddr = a + 4		
2			wAddr = b + 8	uAddr transfers from 1202 to 1204	
3		wAddr transfers from 1202 to 1206	r = a + b	uAddr transfers from 1204 to 1208	
4	w = load(wAddr)		s = 5 + c		u = load(uAddr)
5		w transfers from 1206 to 1202	z = s + r	u transfers from 1208 to 1204	
6			y = w + s	u transfers from 1204 to 1202	
7			x = u + r		

FIG. 14

Table 5					
Time	In tile 1210	Between tiles 1202 and 1210	In tile 1202	Between tiles 1202 and 1204	In tile 1204
1			wAddr = b + 8		
2		wAddr transfers from 1202 to 1206	uAddr = a + 4		
3		wAddr transfers from 1206 to 1210	r = a + b	uAddr transfers from 1202 to 1204	
4	w = load(wAddr)		s = 5 + c		u = load(uAddr)
5		w transfers from 1210 to 1206	z = s + r	u transfers from 1204 to 1202	
6		w transfers from 1206 to 1202	x = u + r		
7			y = w + s		

FIG. 15